REMARKS

In response to the Office Action dated May 27, 2009, Applicant requests consideration of the foregoing amendments and the following remarks. Claims 1, 9, 10, 13, 17, 18, and 22 are amended. Claim 8 is cancelled and claims 5 and 16 were previously cancelled. Claims 1-4, 6, 7, 9-15, and 17-22 are currently pending in the application. No new matter has been added by virtue of the amendments.

I. Claim Rejections - 35 U.S.C. § 103

Rejection of Claims 1-4, 6-7, 9-15, 17, and 22:

Claims 1-4, 6-7, 9-15, 17, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2002/0176489 to Sririam et al. (herein "Sririam") in view of U.S. Patent No. 6,108,693 to Tamura (herein "Tamura"). Applicant has amended claims 1, 9, 10, 13, 17, and 22, from which the remaining rejected claims depend, and respectfully traverses this rejection.

Sririam discloses a vector correlator based Rake receiver that employs a circular buffer (para. [0007]). Two of the three buffers are available for processing by a correlator datapath while the remaining buffer is being written into by incoming chips (para. 0009]). The triple data buffer implements a sliding buffer of 16-chips in which the buffer slides by an interval of 16-chips in a circular fashion in each iteration (FIG. 1 and para. 0040]). At each correlator co-processor (CCP) iteration, 32-chips from the 48-chip triple data input buffer 100 are available for processing by the CCP datapath. At the next iteration, a new set of 16-chips, along with an older set of 16-chips, becomes available to the datapath (FIG. 1 and para. [0040]).

Tamura discloses a system and method of data communication between processors in a multiprocessor system that includes a transmitting processor, a receiving processor, and a shared memory (col. 2, lines 14-18). Two communication buffers are defined in the shared memory, and the transmitting buffer includes communication buffer selecting means for selecting one of the two communication buffers, and write inhibit means for changing the selected communication buffer to a write-disabled state in order to inhibit writing of the selected communication buffer by other processors (col. 2, lines 19-25). The receiving processor includes communication buffer selecting means for selecting one of the two

communication buffers, and read wait means for causing the receiving processor to wait until the selected communication buffer attains a read-enabled state (col. 2, lines 33-40). During the time that the transmitting processor is writing part of a message to a communication buffer, the receiving processor, even though it is capable of reception, cannot read in the message until writing is finished (col. 1, lines 50-58). However, the communication buffer selecting means of the transmitting buffer writes data by alternately selecting first and second communication buffers, and the buffer selecting means of the receiving processor reads in data by alternately selecting the first and second communication buffers (col. 2, lines 46-55).

Applicant's claims 1-4, 6-7, 9-15, 17, and 22 include at least the following features, which differentiate claims 1-4, 6-7, 9-15, 17, and 22 from that which is disclosed by Sririam, Tamura or their combination:

Claim 1:

". . . processing . . . the first digital samples in the first buffer and the second buffer for all known paths of the first group of symbols during a first symbol group duration, wherein the processor is clocked by a processor clock at a clock rate that is faster than and not synchronous with the sample rate;

disabling the processor upon completion of processing the first digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration;

simultaneously with processing the first digital samples, buffering second digital samples corresponding to a second group of symbols into the second buffer and a third buffer, . . . wherein the first symbol group duration represents a duration of time during which the second digital samples are buffered into the second buffer and the third buffer;

at a beginning of a second symbol group duration that occurs consecutively with an end of the first symbol group duration, enabling the processor to process the second digital samples . . ."

Claim 9:

". . . processing . . . during a first symbol group duration, symbols corresponding to a first group of symbols . . ., wherein the first group of symbols in a first path start in a first buffer and end in a second buffer;

receiving samples at a third buffer simultaneously with processing the first group of symbols;

disabling the processor upon completion of processing the symbols corresponding to the first group by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration, wherein the first symbol group duration ends when samples in the third buffer are ready for processing . . ."

Claim 10:

". . . process first digital samples corresponding to a first group of symbols to be processed in a plurality of buffers, the first digital samples starting in a first buffer of the plurality of buffers and ending in a second buffer of the plurality of buffers;

wherein the processing unit processes the first digital samples during a first symbol group duration, and wherein additional digital samples are received at a third buffer of the plurality of buffers simultaneously with the first digital samples being processed, and wherein the first symbol group duration represents a duration of time that ends upon completion of synchronously filling the third buffer with the additional digital samples, and

wherein, prior to an end of the first symbol group duration, the processing unit is disabled upon completion of processing the first digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration."

Claim 13:

". . . processing . . . during a first symbol group duration, the first symbols in the first group of sample buffers while simultaneously communicating additional digital samples from the receiver into a second group of sample buffers during the processing, wherein the additional digital samples include second symbols, and wherein the first symbol group duration represents a duration of time during which the second group of sample buffers is filled with the additional digital samples;

prior to an end of the first symbol group duration, disabling the processor upon completion of processing the first symbols in the first group of sample buffers by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration; and

at a beginning of a second symbol group duration, enabling the processor to process the second symbols in the second group of sample buffers during the second symbol group duration, wherein the beginning of the second symbol group duration occurs consecutively with the end of the first symbol group duration."

Claim 17:

". . . processing, . . . during a first symbol group duration, first samples corresponding to a first group of symbols to be processed, wherein the first samples start in a first buffer and end in a second buffer, and simultaneously receiving second samples at a third buffer during the processing of the first group of symbols, wherein the second samples correspond to a second group of symbols to be processed, and the first symbol group duration represents a duration of time that ends upon completion of synchronously filling the third buffer with the second samples;

prior to an end of the first symbol group duration, disabling the processor upon completion of processing the first samples corresponding to the first group by gating off the processor clock, wherein the processor remains disabled during a remainder of the first symbol group duration . . ."

Claim 22:

". . . processes the first digital samples during a first symbol group duration, and wherein additional digital samples are received at a third buffer of the plurality of buffers simultaneously with the first digital samples being processed, and wherein the processing unit is operable to select digital samples or an intermediate result from a buffer coupled to the processing unit, and

wherein, prior to an end of the first symbol group duration, the processing unit is disabled upon completion of processing the first digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration, and wherein the processor is enabled at a beginning of a second symbol group duration, wherein the end of the first symbol group duration coincides with the beginning of the second symbol group duration."

Neither Sririam, Tamura nor their combination disclose each and every feature of claims 1-4, 6-7, 9-15, 17, and 22. More particularly, none of the references alone or in combination disclose disabling a processor by gating off a processor clock prior to an end of a symbol group duration. In addition, none of the references alone or in combination disclose enabling a processor (that had previously been disabled) at a beginning of a second symbol group duration, where an end of a first symbol group duration coincides with the beginning of the second symbol group duration.

Based on the amendments and the above remarks, Applicant believes that the rejection of claims 1-4, 6-7, 9-15, 17, and 22 under 35 U.S.C. 103(a) has been overcome. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn, and that claims 1-4, 6-7, 9-15, 17, and 22 be allowed.

Rejection of Claim 5:

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam, Tamura, and U.S. Patent No. 6,650,140 to Lee et al. (herein "Lee"). Applicant previously cancelled claim 5, and therefore this rejection is moot.

Rejection of Claim 8:

Claim 8 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam and Tamura in view of U.S. Patent No. 6,714,527 to Kim et al. (herein "Kim"). Applicant has cancelled claim 8, and therefore this rejection is now moot.

Rejection of Claim 16:

Claim 16 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam in view of U.S. Patent Publication No. 2002/0176489 to Roohparvar (herein "Roohparvar"). Applicant previously cancelled claim 16, and therefore this rejection is moot.

Rejection of Claims 18-21:

Claims 18-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam in view of Tamura, and further in view of U.S. Patent Publication No. 2001/0038633 to Robertson et al. (herein "Robertson"). Applicant has amended claim 18, from which the remaining rejected claims depend, and respectfully traverses this rejection.

The Sririam and Tamura references were previously discussed. Robertson discloses a network switch system 10 in which a clock frequency compensation FIFO 34 having a circular buffer 44 is implemented (FIG. 6, and para. [0052]). The circular buffer 44 has five entries, where each entry is associated with an instance of receive/transmit valid logic (FIG. 6, para. [0051]).

Applicant's claims 18-21 include at least the following features, which differentiate claims 18-21 from that which is disclosed by Sririam, Tamura, and Robertson:

". . . processing, by the processor during a first symbol group duration, . . . wherein buffered digital samples corresponding to the first group of symbols start in a first buffer and end in a third buffer, and receiving samples at a fourth buffer and a fifth buffer simultaneously with the first group of symbols being processed;

prior to an end of the first symbol group duration, disabling the processor upon completion of processing the first group of symbols by gating off the processor clock, wherein the processor remains disabled during a remainder of the first symbol group

duration, wherein the end of the first symbol group duration coincides with a beginning of a second symbol group duration . . ."

Neither Sririam, Tamura, Robertson nor their combination discloses each and every feature of claims 18-21. More particularly, none of the references alone or in combination disclose disabling a processor by gating off a processor clock prior to an end of a symbol group duration.

Based on the amendments and the above remarks, Applicant believes that the rejection of claims 18-21 under 35 U.S.C. 103(a) has been overcome. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn, and that claims 18-21 be allowed.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (480) 385-5060. If necessary, the Commissioner is hereby authorized to charge payment or credit any overpayment to Deposit Account No. 50-2091 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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